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Optimal Soft-Switching Scheme for Bidirectional DC-DC Converters with Auxiliary Circuit

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Abstract

This paper proposes a soft-switching bidirectional dc-dc converter (BDC) with an auxiliary circuit. The proposed BDC can achieve the zero-voltage switching (ZVS) using an auxiliary circuit in the buck and boost operations. The auxiliary circuit supplies optimal energy for the ZVS operation of the main switches. The auxiliary circuit consists of a resonant inductor, a back-to-back switch and two capacitors. A small-sized resonant inductor and an auxiliary switch with a low-rated voltage can be used in the auxiliary circuit. Zero-current switching (ZCS) turn-on and turn-off of the auxiliary switches are possible. The proposed soft-switching scheme has a look-up table for optimal switching of the auxiliary switches. The proposed strategy properly adjusts the turn-on time of the auxiliary switch according to the load current. The proposed BDC is verified by the results of PSIM simulations and experiments on a 3-kW ZVS BDC system.

Key words: Auxiliary circuit, Bidirectional dc-dc converter (BDC), Look-up table, Soft switching, Zero-voltage switching

I. INTRODUCTION

As the energy crises continues to accelerate, renewable energy has become the focus of research as a replacement for fossil fuels. In addition, research on power conversion systems (PCSs) such as renewable energy, battery chargers, energy storage systems (ESSs), and electric vehicles (EVs) have increased. In particular, ESSs can be applied to various applications to save and utilize energy efficiently. In order to charge and discharge a battery, a bidirectional dc-dc converter (BDC) is necessary for high reliability, stability, and efficiency [1]-[4].

BDCs are categorized into two types depending on the purpose. The first type is made up of isolated converters [5]-[7] and the other type includes non-isolated converters [8]-[10]. An isolated BDC can protect a system by separating its input and output stages from the transformer located between the primary and secondary sides. Therefore, isolated dc-dc converters are widely used in many applications requiring galvanic isolation. However, isolated converters have a complex structure that increases the cost and volume of a system due to the transformer and the number of the power switches. On the other hand, non-isolated converters have a simple structure without galvanic isolation. This converter configuration is possible at a low cost and a small volume. However, these converters have the disadvantage of high stress on the power switches due to hard switching.

For this reason, a number of studies on soft switching have been conducted to obtain high-efficiency non-isolated converters [11]-[14]. The basic half-bridge type BDC was proposed in [11] to achieve soft switching. Since a BDC should be designed at its rated power to achieve ZVS operation, the efficiency of light loads decreases due to a large current ripple. A half-bridge bidirectional dc-dc converter with a few passive components was proposed in [12] to improve system efficiency. However, the proposed topology has disadvantages due to the complex design of its passive components and control strategy. Many passive components and switching devices were added in [13] to accomplish the ZVS operation. Excessive current is required in the additional circuit for the ZVS operation. This results in current stress on the power devices.

In this paper, a soft switching bidirectional dc-dc converter with an auxiliary circuit is proposed. An auxiliary circuit is

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added to a conventional half-bridge BDC for ZVS operation in the buck and boost modes. The auxiliary circuit consists of a resonant inductor, a back-to-back switch and two capacitors. When compared to conventional topologies, the auxiliary circuit of the proposed converter has a simple structure and control method. Power switches with a low-rated voltage can be used in the auxiliary circuit. The power losses of the auxiliary switches are minimized by the zero-current switching (ZCS) operation. The proposed BDC is verified by the results of PSIM simulations and experiments on a 3-kW ZVS BDC system.

II. Description of the Proposed Bidirectional DC-DC Converter

A. Configuration of the Proposed Converter

The proposed ZVS BDC is shown in Fig. 1. The topology is configured by adding an auxiliary circuit to a half-bridge BDC. The auxiliary circuit comprises a resonant inductor, a back-to-back switch and two capacitors. The switches S_1 and S_2, which operate as main switches, transfer power in both directions and are complementary to each other. The auxiliary circuit is used to supply the minimum ZVS energy to the main switches. The turn-on time of the auxiliary switches is adjusted by a look-up table, which is made offline depending on the load current. The proposed ZVS BDC can be operated in both the buck and boost operation.

B. Analysis of Buck Operation

Fig. 3 shows a key waveform of the proposed ZVS BDC during one switching period of buck operation. The waveform is divided into eight modes depending on the switching state. Fig. 2 shows equivalent circuits of the proposed ZVS BDC during the buck mode.

Mode 1 [t_0–t_1]: At t = t0, the buck switch (S_1) is in the turn-on state and the other switches are all in the turn-off state. When the auxiliary switch (S_{A2}) is turned on, Mode 1 is started. The ZCS turn-on of S_{A2} is possible due to the switching operation at the zero current. Because positive voltage (V_{high} - V_{low}) is supplied to the filter inductor, the filter inductor current (I_{Lf}) is increased in the positive direction. On the other hand, the resonant inductor current (I_{Lr}) is increased in the negative direction due to the negative voltage across the resonant inductor. The negative resonant inductor current flows to C_{top} and C_{bot}, and the voltage of C_{bot} is increased during Mode 1. The voltage of C_{bot} is maintained at half of V_{high}. When S_1 is turned off, Mode 1 is finished. The equations for Mode 1 are described as:

$$i_{Lf}(t_0) = I_{Lf\_0},\ \ i_{Lr}(t_0) = I_{Lr\_0} = 0 \tag{1}$$

$$v_{Cr1}(t_0) = 0,\ \ v_{Cr2}(t_0) = V_{high} \tag{2}$$

$$i_{Lf}(t) = \frac{1}{L_f}\left(V_{high} - V_{low}\right)(t_1 - t_0) + I_{Lf\_0} \tag{3}$$

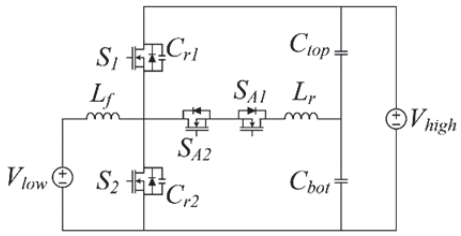


Fig. 1. Proposed ZVS bidirectional dc-dc converter.

$$i_{Lr}(t) = -\frac{1}{2L_r}V_{high}(t_1 - t_0) \tag{4}$$

$$i_{Lf}(t_1) = I_{Lf\_1},\ \ i_{Lr}(t_1) = I_{Lr\_1} \tag{5}$$

Mode 2 [t_1–t_2]: When S_1 is turned off, Mode 2 begins. In this mode, two steps are performed during the dead-time. During the first step, the upper resonant capacitor (C_{r1}) is charged and the lower resonant capacitor (C_{r2}) is discharged by the resonance. Therefore, the ZVS condition of S_2 is satisfied when the voltage of C_{r2} reaches zero. When the first step is finished, the filter and the resonant inductor current are decreased by flowing through the anti-parallel diode of the boost switch (S_2). The equations for this mode are shown in (6)-(12). ω_r is the resonant angular frequency and Z_r is the characteristic impedance. When S_2 is turned on, this mode is finished.

$$v_{Cr1}(t_1) = 0,\ \ v_{Cr2}(t_1) = V_{high} \tag{6}$$

$$i_{Lr}(t) = I_{Lr\_1} + \frac{V_{high}}{2Z_r}\sin\omega_r(t - t_1) \tag{7}$$

$$v_{Cr1}(t) = \frac{1}{C_{r1}}\left(i_{Lf} - i_{Lr}\right)(t - t_1) \tag{8}$$

$$v_{Cr2}(t) = V_{high} - \frac{1}{C_{r2}}\left(i_{Lf} - i_{Lr}\right)(t - t_1) \tag{9}$$

$$C_r = C_{r1} + C_{r2} \tag{10}$$

$$V_{Cr1}(t_2) = V_{high},\ \ V_{Cr2}(t_2) = 0 \tag{11}$$

$$\omega_r = \frac{1}{\sqrt{L_r C_r}},\ \ Z_r = \sqrt{\frac{L_r}{C_r}} \tag{12}$$

Mode 3 [t_2–t_3]: When S_2 is turned on, Mode 3 starts. Because I_{Lf} and I_{Lr} flow through the anti-parallel diode of S_2, I_{Lf} and I_{Lr} decrease continuously in this mode. When I_{Lr} reaches zero, only I_{Lf} flows into the anti-parallel diode of S_2. The ZCS turn-off of S_{A2} is possible because S_{A2} is turned off when I_{Lr} reaches zero. The equations for this mode are shown in (13)-(16). When S_{A2} is turned off, Mode 3 is finished.

$$i_{Lf}(t_2) = I_{Lf\_2},\ \ i_{Lr}(t_2) = I_{Lr\_2} \tag{13}$$

$$i_{Lf}(t) = I_{Lf\_2} - \frac{V_{low}}{L_f}(t_3 - t_2) \tag{14}$$

$$i_{Lr}(t) \simeq I_{Lr\_2} + \frac{V_{high}}{2L_r}(t - t_2) \tag{15}$$

$$i_{Lf}(t_3) = I_{Lf\_3},\ \ i_{Lr}(t_3) = 0 \tag{16}$$

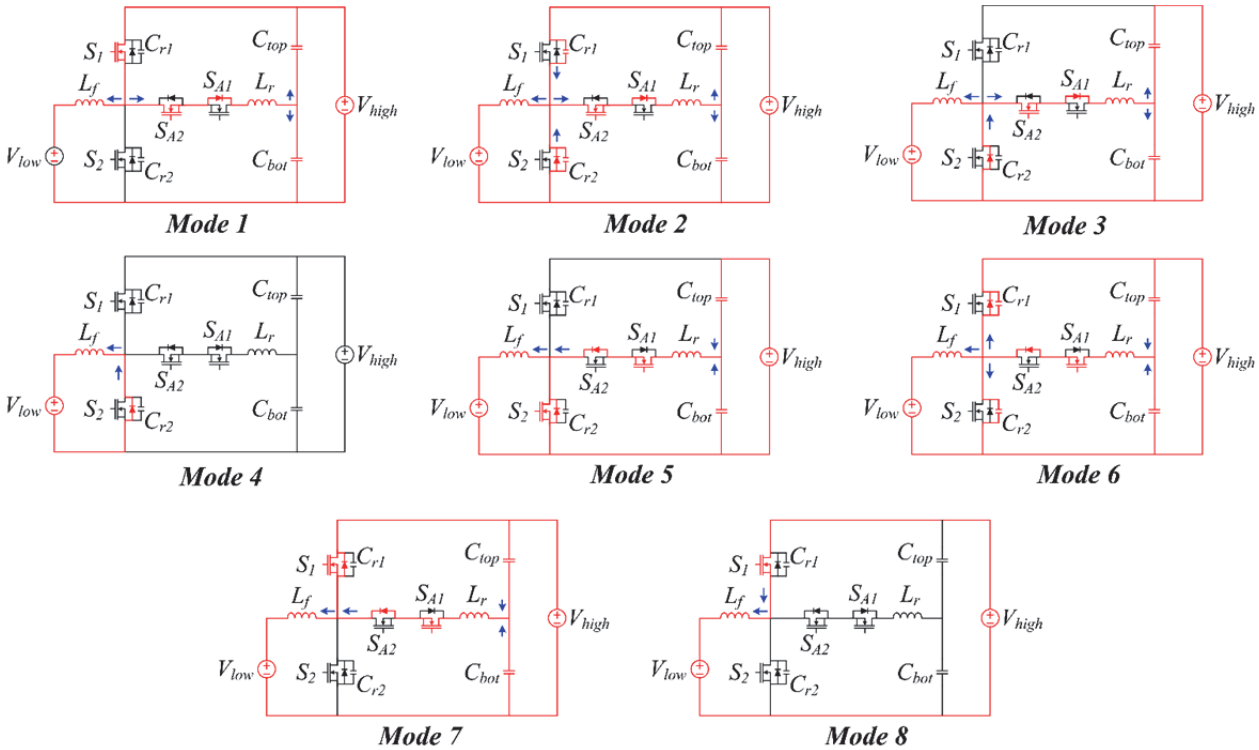


Fig. 2. Equivalent circuits of the ZVS BDC in the buck mode.

Mode 4 [t_3–t_4]: When S_{A2} is turned off, Mode 4 is activated. In Mode 4, I_{Lf} flows into the anti-parallel diode of S_2 until the auxiliary switch (S_{A1}) is turned on, as shown by:

$$i_{Lr}(t) = 0 \tag{17}$$

$$i_{Lf}(t) = I_{Lf\_3} - \frac{V_{low}}{L_f}(t_4 - t_3) \tag{18}$$

$$i_{Lf}(t_4) = I_{Lf\_4}, \quad i_{Lr}(t_4) = 0 \tag{19}$$

Mode 5 [t_4–t_5]: At $t = t_4$, S_2 is in turn-on state and the other switches are all in the turn-off state. When the auxiliary switch S_{A1} is turned on, Mode 5 is started. The ZCS turn-on of S_{A1} is possible in the same manner as in Mode 1. Because the voltage across the filter inductor is negative ($-V_{low}$), I_{Lf} is decreased. When the auxiliary switch S_{A1} is turned on, I_{Lr} begins to gradually increase. Until I_{Lr} is smaller than I_{Lf}, the difference between I_{Lf} and I_{Lr} flows to the anti-parallel diode of S_2. After I_{Lr} is larger than I_{Lf}, the difference between I_{Lr} and I_{Lf} flows through the transistor of S_2. The equations for this mode are shown in (20)-(24). When S_2 is turned off, Mode 5 is finished.

$$i_{Lf}(t) = I_{Lf\_4} - \frac{V_{low}}{L_f}(t_5 - t_4) \tag{20}$$

$$i_{Lr}(t) = \frac{V_{high}}{2L_f}(t_5 - t_4) \tag{21}$$

$$i_{Lf}(t_5) = I_{Lf\_5} \simeq I_{Lf,\min} \tag{22}$$

$$i_{Lr}(t_5) = I_{Lr\_5} \simeq I_{Lr,\max} \tag{23}$$

$$v_{Cr1}(t_5) = V_{high}, \quad v_{Cr2}(t_5) = 0 \tag{24}$$

Mode 6 [t_5–t_6]: At $t = t_5$, I_{Lf} and I_{Lr} almost reach their minimum and maximum values, respectively. During the dead-time in which the main switches are turned off, C_{r1} is discharged and C_{r2} is charged by the resonance. When the energy stored in C_{r2} is discharged, the voltage of S_1 (V_{S1}) reaches zero. The ZVS condition of the buck switch is ensured when V_{s1} is zero. After V_{S1} reaches zero, the difference between I_{Lf} and I_{Lr} flows into the anti-parallel diode of S_1. When S_1 is turned on, Mode 6 is finished. The equations for this mode are shown in (25)-(27), and the ZVS energy can be expressed as (28).

$$i_{Lr}(t) = I_{Lr\_5} - \frac{V_{high}}{2L_r}\sin\omega_r(t - t_5) \tag{25}$$

$$v_{Cr1}(t) = V_{high} - \frac{1}{2C_{r1}}\left(i_{Lr} - i_{Lf}\right)(t - t_5) \tag{26}$$

$$v_{Cr2}(t) = \frac{1}{2C_{r1}}\left(i_{Lr} - i_{Lf}\right)(t - t_5) \tag{27}$$

$$\frac{1}{2}L_r{I_{Lr}}^2 \geq \frac{1}{2}(C_{r1} + C_{r2}){V_{high}}^2 \tag{28}$$

Mode 7 [t_6–t_7]: When S_1 is turned on, Mode 7 is activated. Current equal to the difference between I_{Lf} and I_{Lr} flows into the anti-parallel diode of S_1 until I_{Lf} is larger than I_{Lr}. When I_{Lf} is larger than I_{Lr}, current equal to the difference between I_{Lf} and I_{Lr} flows into the transistor of S_1. In this mode, I_{Lr} decreases and reaches zero. S_{A1} is operated under ZCS turn-off at this moment. This exquations for this mode ar described in (29)–(32). When S_{A1} is turned off, Mode 7 is finished.

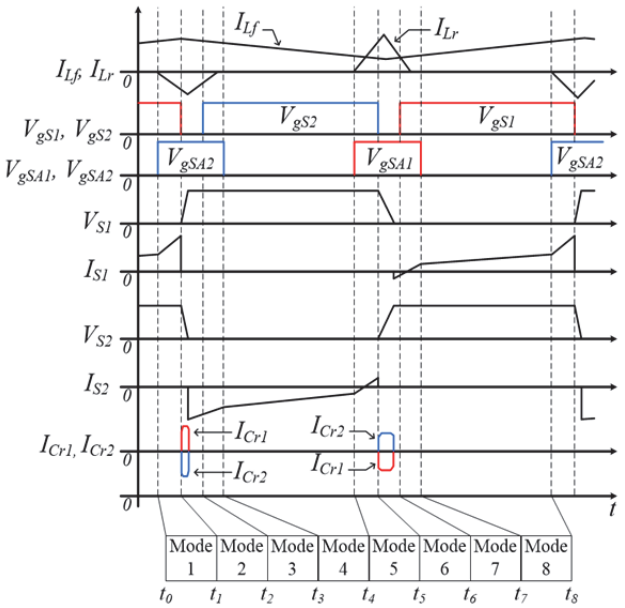


Fig. 3. Key waveform in buck operation.

$$i_{Lf}(t_6) = I_{Lf\_6},\ \ i_{Lr}(t_6) = I_{Lr\_6} \tag{29}$$

$$i_{Lf}(t) = I_{Lf\_6} + \frac{V_{high} - V_{low}}{L_f}(t_7 - t_6) \tag{30}$$

$$i_{Lr}(t) = I_{Lr\_6} - \frac{V_{low}}{2L_r}(t - t_6) \tag{31}$$

$$i_{Lf}(t_7) = I_{Lr\_7},\ \ i_{Lr}(t_7) = 0 \tag{32}$$

Mode 8 [t_7–t_8]: Mode 8 starts when S_{A1} is tuned off. I_{Lf} flows through the filter inductor from V_{high} to V_{low}. Because positive voltage is supplied to the filter inductor, I_{Lf} increases linearly. I_{Lf} is described as (33). In Mode 8, the converter transfers power from V_{high} to V_{low}. At the end of Mode 8, I_{Lf} has its maximum value, I_{Lf}, max.

$$i_{Lf}(t) = I_{Lr\_7} + \frac{V_{high} - V_{low}}{L_f}(t_8 - t_7) \tag{33}$$

C. Analysis of Boost Operation

Fig. 3 shows key waveform of the proposed ZVS BDC during one switching period of buck operation. The waveform is divided into eight modes depending on the switching state. Fig. 2 shows an equivalent circuit of the proposed ZVS BDC during the buck mode.

Boost mode operation can also be divided into eight modes. However, the roles of the switches are opposite. S_2 and S_1 act as the main switches. Meanwhile, the auxiliary switches are also changed in the boost mode operation. S_{A2} supplies ZVS energy to S_2, and S_{A1} helps maintain the voltage of C_{bot} at half of V_{high}. Fig. 5 shows a key waveform of the proposed ZVS BDC during one switching period in the boost mode. An equivalent circuit of the proposed ZVS BDC is shown in Fig. 4 during boost operation.

III. Design Method of the Circuit Parameters

A. Design of the Filter Inductance

The design of the filter inductance has a significant impact on the performance of the proposed BDC. The current of the resonant inductor should be large to achieve ZVS operation with a large filter inductance. In this case, the large current of the resonant inductor increases the conduction loss of the auxiliary switches. On the other hand, with a small filter inductance, the main switches have a large current stress due to a large current ripple. Therefore, the filter inductance must be designed first.

In this paper, the target of the filter inductor current ripple is less than 40 % of the rated load current. ΔI_{Lf} can be expressed as (34).

$$\Delta i_{Lf} = \frac{V_{high} - V_{low}}{L_f} \times D_m T_s < I_{rated} \times 0.4 \tag{34}$$

where D_m is the duty ratio of the main switch, T_s is the switching period, V_{high} is the high-voltage, V_{low} is the low-voltage, and L_f is the filter inductance. Using (34), the filter inductance can be derived as (35).

$$L_f > \frac{V_{high} - V_{low}}{\Delta i_{Lf}} \times D_m T_s \tag{35}$$

B. Design of the Resonant Inductance

To achiever ZVS operation, $i_{Lr,max}$ should be larger than $i_{Lf,min}$. In buck operation, I_{Lf} is equal to the load current. Therefore, I_{Lf} can be expressed as (36).

$$I_{Lf} = \frac{P_{Load}}{V_{low}} \tag{36}$$

where P_{Load} is the power of a specific load condition. Using (34) and (36), $i_{Lf,min}$ can be expressed as:

$$\begin{aligned} i_{Lf,\min} &= I_{Lf} - \frac{\Delta i_{Lf}}{2} \\ &= \frac{P_{Load}}{V_{low}} - \frac{V_{high} - V_{low}}{2 \times L_f} \times D_m T_s \end{aligned} \tag{37}$$

From the inductor current equation, $i_{Lr,max}$ can be expressed as (38).

$$i_{Lr,\max} = \frac{V_{high}}{2 \times L_r} \times T_{alpha} \tag{38}$$

T_{alpha} should be limited to within 5 % of the switching period. T_{alpha} can be expressed as (39). From equations (38) and (39), the resonant inductance can be derived as (40).

$$T_{alpha} < T_s \times 0.05 \tag{39}$$

$$L_r < \frac{V_{high} \times T_{alpha}}{2 \times i_{Lf,\min}} \tag{40}$$

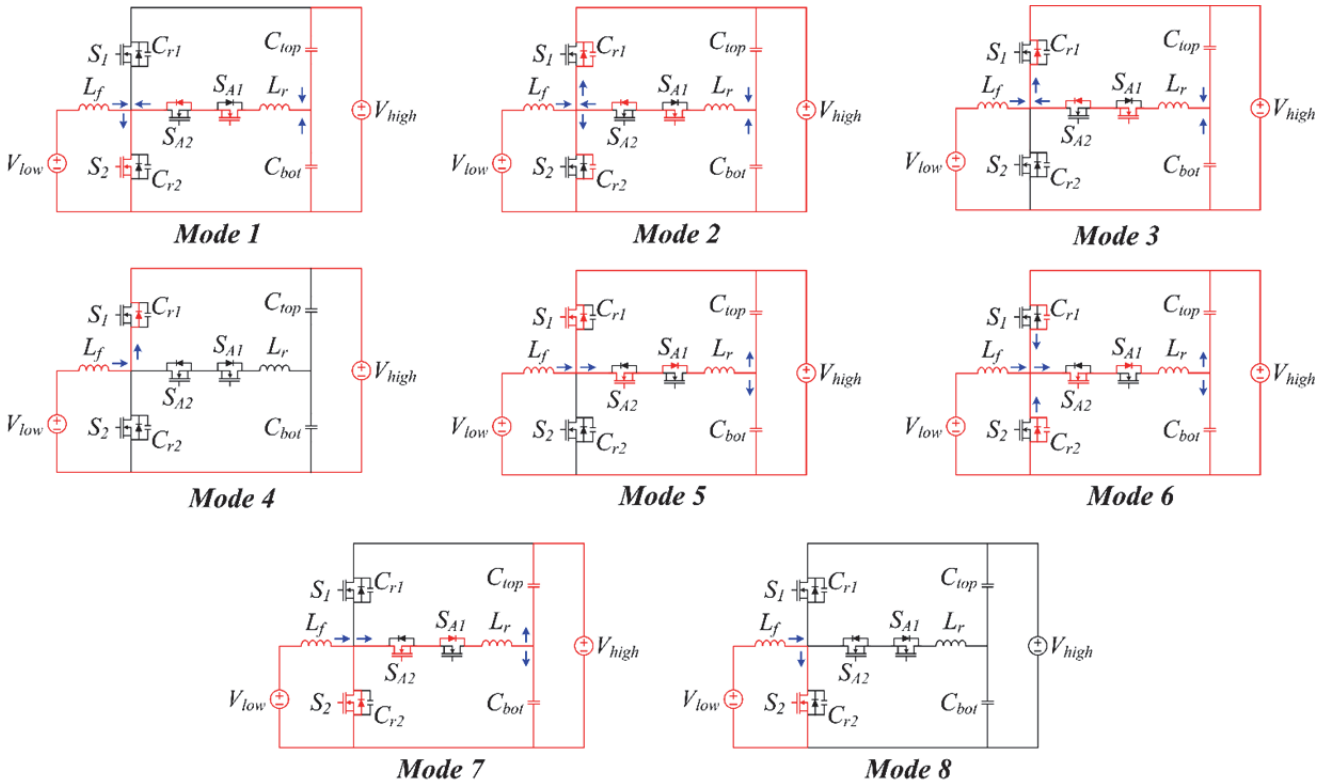


Fig. 4. Equivalent circuits of the ZVS BDC in the boost mode.

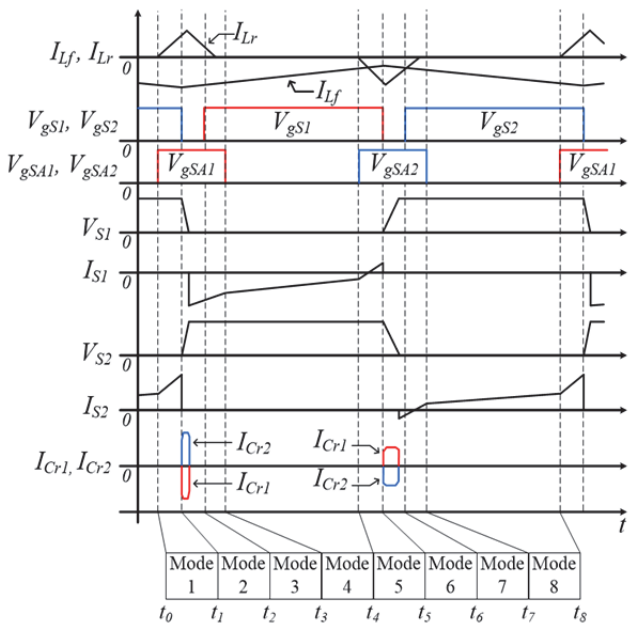


Fig. 5. Key waveform in boost operation.

C. Design of the Resonant Capacitor

Typically, an additional capacitor achieves a greater reduction in the turn-off loss. The turn-off loss and the conduction loss are inversely proportional to each other. When the resonant capacitance is large, the turn-off loss of the main switches is decreased. However, the conduction loss of the main switch is increased due to the large current of the resonant inductor. In the opposite case, with a small resonant capacitance, the turn-off loss is increased and the conduction loss is decreased. Therefore, an optimal design method for the resonant capacitor is needed to minimize the total loss of the main switches. A power loss analysis of the PSIM simulation tools is used to design the resonant capacitor in this paper. The result of a PSIM simulation is presented to choose a proper resonant capacitance in the design example section.

IV. Control Algorithm of the Proposed Topology

A. Description of the Control Algorithm

Fig. 6 shows a block diagram of the proposed control algorithm. The duty of the main switches, which is generated from the current controller, is compared with V_{tri1}, and the power is transferred in both directions. The duty of the auxiliary switch depending on the load is determined by a look-up table. In addition, two phase shifted carrier waves are generated to compare with the duty ratio of the auxiliary switches. V_{tri2} lags V_{tri1} by half the duty of S_1. On the other hand, V_{tri3} leads V_{tri1} by half the duty of S_2. In buck operation, the duty of S_{A1} is compared with V_{tri2} to generate the ZVS energy for S_1. On the other hand, S_{A2} is used to maintain V_{Cbot} at half of V_{high}. When only S_{A1} is operated, V_{Cbot} continuously

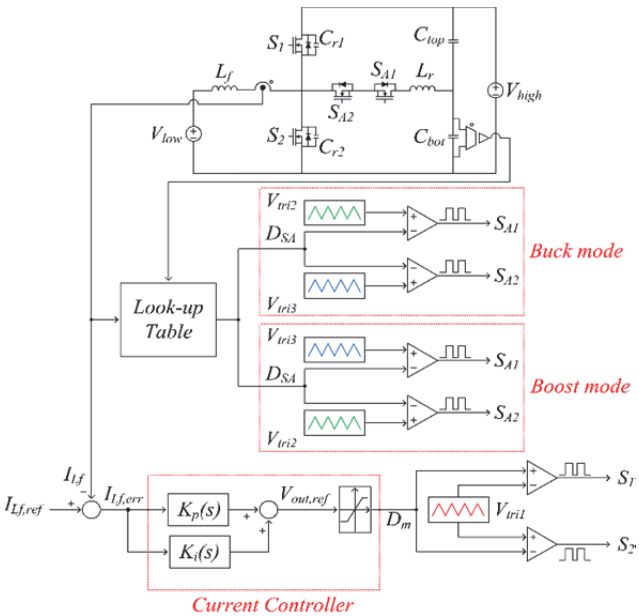


Fig. 6. Block diagram of the proposed control algorithm.

decreases, resulting in an unbalance between V_{Ctop} and V_{Cbot} on the high-voltage side. In this case, the ZVS operation of the main switches cannot be achieved because the energy stored in the resonant inductor is not sufficient. To solve this problem, the operation of S_{A2} is required. The phase shift method of the two carrier waves (V_{tri2} and V_{tri3}) and the method for calculating the duty of the auxiliary switch are described in the next section. In boost operation, the role of the auxiliary switches is opposite. S_{A2} is triggered for the ZVS operation of S_2, and S_{A1} is used to maintain V_{Cbot} at half of V_{high}.

B. Minimizing the Switching Loss with a Look-Up Table

It is difficult to obtain resonant current data due to DSP performance limitations. Therefore, in this study, a look-up table is used to reduce the operation time and to provide the duty of the auxiliary switch according to each load current. To achieve the ZVS operation of the main switches, an optimal resonant current is injected. In order to generate the minimum resonant inductor current, the optimal turn-on time of the auxiliary switch needs to be calculated. It is possible to obtain the optimal turn-on time under the assumption that some of the parameters are known.

Fig. 7 shows a method for calculating the turn-on time of the auxiliary switch. It is assumed that the energy stored in C_{r1} is discharged completely during the dead-time of the auxiliary switch in buck operation. To obtain the optimal turn-on time of the auxiliary switches, the minimum value of I_{Lf} and the maximum value of I_{Lr} need to be known. As mentioned previously, during the dead-time, the current difference between I_{Lr} and I_{Lf} charges and discharges the resonant capacitors. For buck operation, the average value of I_{Lf} is equal to the load current.

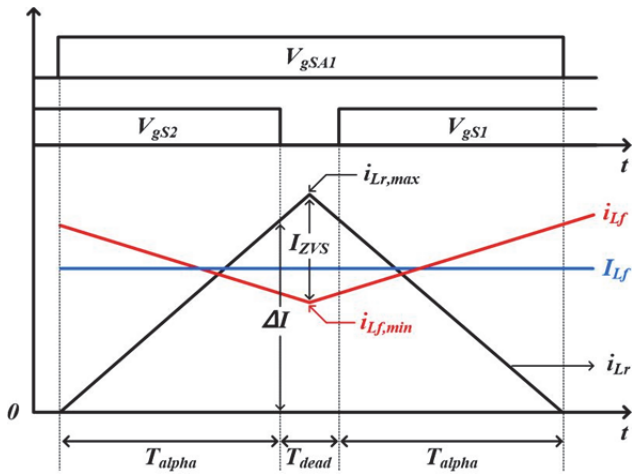


Fig. 7. I_{Lf} and I_{Lr} depending on the PWM signal of the main and auxiliary switches.

When S_2 is turned off, as shown in Fig. 7, I_{Lr} can be approximated to a maximum value since there is almost no difference between $i_{Lr,max}$ and ΔI during the dead-time. Therefore, the maximum value of I_{Lr} can be approximated as:

$$I_{Lr,\max} \simeq \frac{V_{Lr} \times T_{alpha}}{L_r} = \frac{V_{high} \times T_{alpha}}{2L_r} \tag{41}$$

The current for the ZVS operation (I_{ZVS}) can be expressed as:

$$I_{ZVS} = I_{Lr,\max} - I_{Lf,\min} \tag{42}$$

$$I_{ZVS} = \frac{V_{high} \times T_{alpha}}{2L_r} - \left(\frac{P_{Load}}{V_{low}} - \frac{V_{high} - V_{low}}{2L_f} \times D_m T_s \right) \tag{43}$$

In this study, the resonant capacitors are assumed to be fully charged and discharged during the dead-time, and I_{ZVS} is assumed to be a constant value because the dead-time is extremely short. Therefore, from the voltage equation of the capacitor, I_{ZVS} is expressed as:

$$I = 2 \times C_r \frac{dV_c}{dt} \tag{44}$$

$$I_{ZVS} = 2C_r \frac{V_{high}}{T_{dead}} \tag{45}$$

From (43) and (45), T_{alpha} can be derived as:

$$T_{alpha} = \left(2C_r \frac{V_{high}}{T_{dead}} + \left(\frac{P_{Load}}{V_{low}} - \frac{V_{high} - V_{low}}{2L_f} \times D_m T_s \right) \right) \times \frac{2L_r}{V_{high}} \tag{46}$$

The optimal turn-on time of the auxiliary switch (T_{aux}) is equal to equation (47) as shown in Fig. 7. Therefore, the optimal duty of the auxiliary switch (D_{aux}) can be expressed as:

$$T_{aux\_sw\_on} = 2 \times T_{alpha} + T_{dead} \tag{47}$$

$$D_{aux} = \frac{T_{aux\_sw\_on}}{T_s} \tag{48}$$

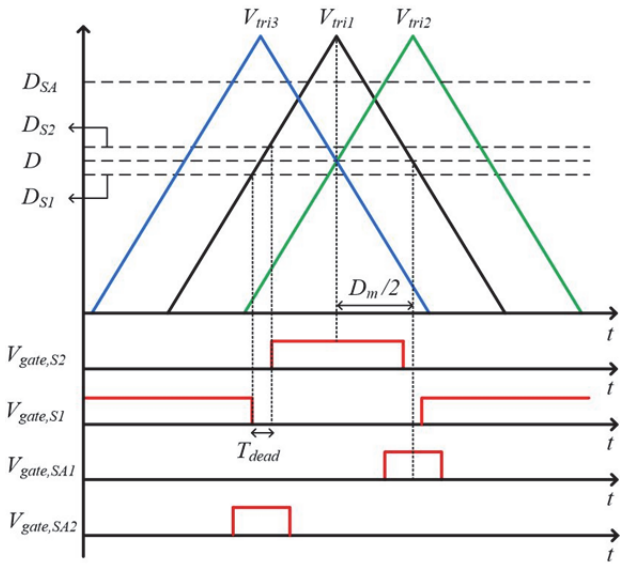


Fig. 8. Phase shift method for the switching operation.

T_{alpha} is determined by P_{load} in (46). Therefore, (48) always has an optimal value with a variation of the load. D_{aux} is calculated with the entire load offline and is saved to the look-up table. A minimal I_{Lr} is used because the resonant capacitors are charged and discharged during the dead-time. Therefore, the power loss of the auxiliary circuit can be minimized. The auxiliary switches remain in the turn-on state while one of the main switches S_1 or S_2 is turned on. Thus, $T_{aux\_sw\_on}$ should be smaller than the turn-on time of the main switch. The available duty ratio can be expressed as:

$$\begin{aligned} T_{aux\_sw\_on} &< (1-D_m)T_s \qquad (D_m > 0.5) \\ T_{aux\_sw\_on} &< D_m T_s \qquad (D_m < 0.5) \end{aligned} \tag{49}$$

In the proposed control algorithm, three up-down carrier waves are used to operate the main and auxiliary switches. A phase shift method for the operation of the auxiliary switches is proposed in this paper. Fig. 8 shows this phase shift method.

As shown in Fig. 6, the current controller generates the duty of the main switch, and the dead-time is applied to the duty. The duty, including the dead-time, is compared with V_{tri1} to generate a pulse width modulation (PWM) signal. In buck operation, the phase of V_{tri2} lags V_{tri1} by half the duty of the main switch (D_{S2}), and the phase of V_{tri3} leads V_{tri1} by half the duty of the main switch (D_{S1}).

D_{aux} in the look-up table is compared with V_{tri2} or V_{tri3} to generate a PWM signal according to the operation mode. For buck operation, the duty of S_{A1} (D_{aux}) is compared with V_{tri2}, and S_{A1} is operated to perform ZVS of S_1. When only S_{A1} is operated, V_{Cbot} continuously decreases. This results in an unbalance between V_{Ctop} and V_{Cbot}. To solve this problem, under ideal conditions, the duty of S_{A1} is used as the duty of S_{A2}. However, under non-ideal conditions, when the duty of S_{A1} and S_{A2} are the same, the unbalance problem still exists. Therefore, if V_{Ctop} is larger than V_{Cbot}, a duty as small as 1 % of the D_{SA1} duty is used as D_{SA2}. In the opposite case, a duty as large as 1 % of D_{SA1} is used as the S_{A2} duty. For boost operation, the duty of S_{A2} (D_{aux}) is compared with V_{tri3}, and S_{A2} is operated to perform ZVS of S_2. The duty of S_{A1} is determined in the same manner as in buck mode operation.

C. Comparison with Other Topologies

Table I shows a comparison of the proposed topology with other topologies that perform soft switching. In [11], the design of a soft-switching BDC for a high-power system was proposed using the discontinuous conducting mode. The proposed converter has the advantages of simple construction, and reduced turn-off losses by connecting a resonant capacitor. The ZVS operation of the proposed converter can be achieved by using the discontinuous current mode (DCM). The current ripple of the filter inductor should be large enough to meet the DCM condition. Furthermore, the circuit parameters of the dc-dc converter are designed based on the rated power. As a result, the efficiency is decreased under light load conditions since the conduction loss increases due to a large current ripple. Therefore, the current stress of the switches is increased due to a large current ripple.

In [12], a soft switching bidirectional dc-dc converter with an LC series resonant circuit was proposed. The merit of this topology is that the configuration of the system is simple. However, it has drawbacks since the design of the passive components is complicated and the switching frequency changes according to the load condition. The ZVS principle of the proposed BDC is based on the series resonance between the resonant inductor and the capacitor during the turn-off time of the switch. The current generated by the LC resonance flows to the switch during most of the time that the switch is turned on. Therefore, this operation results in a large conduction loss, which leads to a large current stress of the switch.

In [13], a dc-dc converter was proposed that uses an auxiliary resonant circuit. The auxiliary circuit consists of two diodes, two switches, and two passive components. Although the efficiency of the system is increased by reducing the switching loss through soft switching, the configuration and control method are complicated. The ZVS operation is achieved using the auxiliary circuit. The voltage stress is applied to the auxiliary switch with a maximum V_{high}. The large current generated by the resonance flows to the main switch for a long time when compared with one switching period. Therefore, the current flowing to the main switch increases the conduction loss.

In this paper, a soft-switching BDC with an auxiliary circuit and a control algorithm are proposed. Although the system is complex in configuration, the minimum ZVS energy is generated by properaly adjusting the auxiliary switch. The ZVS operation is performed by injecting the

TABLE I
COMPARISON OF DIFFERENT TOPOLOGIES

	[11]	[12]	[13]	Proposed Topology
System configuration	Simple	Simple	Complicated	Complicated
Control method complexity	Simple	Complicated	Simple	Simple
Number of external diodes	0	0	2	0
Number of external switches	0	0	2	2
Number of external passive components	0	3	2	3
Considering the load conditions	Not considered	Considered	Considered	Considered
Voltage stress of the auxiliary switches	No auxiliary switches	No auxiliary switches	Maximum V_{high}	Maximum $V_{high}/2$
Current stress of the switches	Excessive	Large	Large	Small
Efficiency	96.77 %	97.52 %	96.03 %	98.8 %

minimum current during the dead-time. The resonant inductor current flows for a short time when compared with one switching period. The on-time of the auxiliary switch is about 5 μs and the switching period is 40 μs under the experimental conditions. Therefore, the current stress of the auxiliary switches is small due to the low conduction loss of the auxiliary switches. Furthermore, the voltage stress of the auxiliary switch is applied up to half of V_{high}. In terms of the current stress for the switches, the resonant inductor current flows to the main switches during T_{alpha}. Since the maximum value of T_{alpha} should be 2 μs under the experimental conditions, the current stress of the switches is low. In addition, the conduction loss of the auxiliary switches is small.

V. DESIGN EXAMPLE

Based on the design methods, a design example of the passive components is presented. V_{high} is 350 V, V_{low} is 200 V, and f_s is 25 kHz. From the derived equation (34), the filter inductor current ripple can be found as:

$$\Delta i_{Lf} = \frac{350V - 200V}{L_f} \times \frac{200V}{350V} \times 40\mu s < 6 \text{ [A]} \quad (50)$$

Using (35) and (50), the filter inductance is estimated as:

$$L_f > \frac{350V - 200V}{6A} \times \frac{200V}{350V} \times \frac{1}{25kHz} = 571\mu H \quad (51)$$

From equation (51), the filter inductance is selected as 600 μH. Then, the filter inductor current ripple can be calculated as:

$$\Delta i_{Lf} = \frac{350V - 200V}{600\mu H} \times \frac{200V}{350V} \times 40\mu s = 5.71A \quad (52)$$

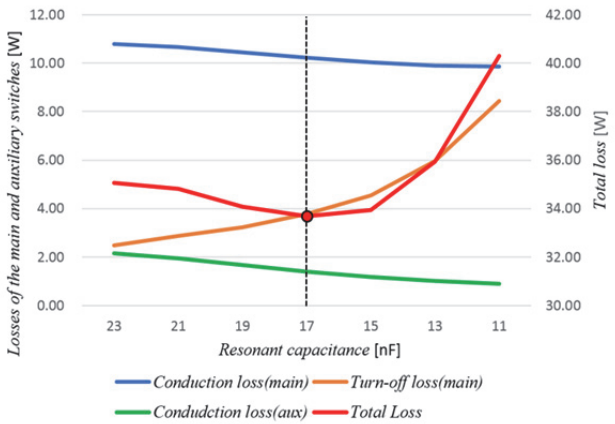


Fig. 9. Loss comparison depending on the resonant capacitance.

When considering the rated power condition, from the derived equations (36) and (37), $i_{Lf,min}$ can be calculated as:

$$i_{Lf,\min} = \frac{3kW}{200V} - \frac{\Delta i_{Lf}}{2} = 12.14A \quad (53)$$

Since the switching frequency is selected as 25 *kHz*, T_{alpha} is selected to be 2 μs by (39). Using (40), the resonant inductance can be evaluated as:

$$L_r < \frac{350V \times 2\mu s}{2 \times i_{Lf,\min}} = 28.8\mu H \quad (54)$$

When considering the volume of the resonant inductor, the resonant inductance is selected as 12 μH.

To design the optimal resonant capacitance, the power loss of the switch is analyzed by a PSIM simulation. Fig. 9 shows a comparison of the losses in terms of the resonant capacitance. Depending on the resonant capacitance, there is a trade-off between the switching loss and the conduction. When the resonant capacitance increases, the turn-off loss

decreases and the conduction loss increases. In the obtained simulation results, when there is a resonant capacitance of 17 *nF*, the total loss is the lowest when compared to the other resonant capacitances. Therefore, 17 *nF* of the resonant capacitor is applied to the proposed BDC.

VI. Simulation Results

Simulations were performed to verify the effectiveness of the proposed ZVS BDC and control algorithm using PSIM software. Table II shows the parameters of the simulation. As previously mentioned, the duty of the auxiliary switch is applied by a look-up table depending one the load conditions.

A. Simulation Results in Buck Operation

Fig. 10 shows simulation results with the proposed control algorithm in buck operation. The phase of V_{tri2}, which is compared with the duty of S_{A1}, lags that of V_{tri1} by half the duty of the main switch. The duty of S_{A1} is referenced in the look-up table. V_{tri3}, which is compared with the duty of S_{A2}, leads V_{tri1} by half the duty of the main switches. The duty of S_{A2} is adjusted to maintain V_{Cbot} at half of V_{high}. When S_2 is turned off, I_{Lr} charges C_{r2} and discharges C_{r1} during the dead-time. V_{S1} reaches zero and remains there during the dead-time. Therefore, the ZVS operation of S_1 can be achieved. In the buck mode, S_{A2} is operated to balance V_{Ctop} and V_{Cbot}.

Fig. 11 shows an analysis of the power losses of the switches. This analysis of the power losses is obtained from a PSIM simulation. As shown in Fig. 11, the power loss from the main switch accounts for 77 % of the total power loss. Of this, the conduction loss of the main switches is dominant. Since the turn-on ZVS operation is performed, the switching loss of the main switches corresponds to the turn-off loss. The power loss generated by the auxiliary switches accounts for 22 % of the total power loss. Since the ZCS turn-on and turn-off operations are performed in the auxiliary switches, most of the power loss generated from the auxiliary switch is conduction loss. The conduction loss and switching loss of the auxiliary switches are 21 % and 1 % of the total loss, respectively.

B. Simulation Results in Boost Operation

Fig. 12 shows the performance and control algorithm of the proposed converter in the boost mode. The phase of V_{tri3} is compared with the duty of S_{A2} to generate a PWM signal of the main switch. The duty of S_{A2} is obtained by a look-up table reference. The phase of V_{tri2}, which is compared with the duty of S_{A1}, leads that of V_{tri1} by the duty of the main switches. The duty of S_{A1} is adjusted to maintain V_{Cbot} at half of V_{high}. With S_{A2} turned on, I_{Lr} is increased linearly. When S_1 is turned off, I_{Lr} charges C_{r1} and discharges C_{r2} during the dead-time. The ZVS condition is satisfied when VC_{r2} is zero,

TABLE II
Proposed ZVS BDC Parameters

Rated power	3 kW
High-side voltage	350 V
Low-side voltage	200 V
Filter inductor	600 μH
Resonant inductor	12 μH
Resonant capacitor	17 nF
Switching frequency	25 kHz

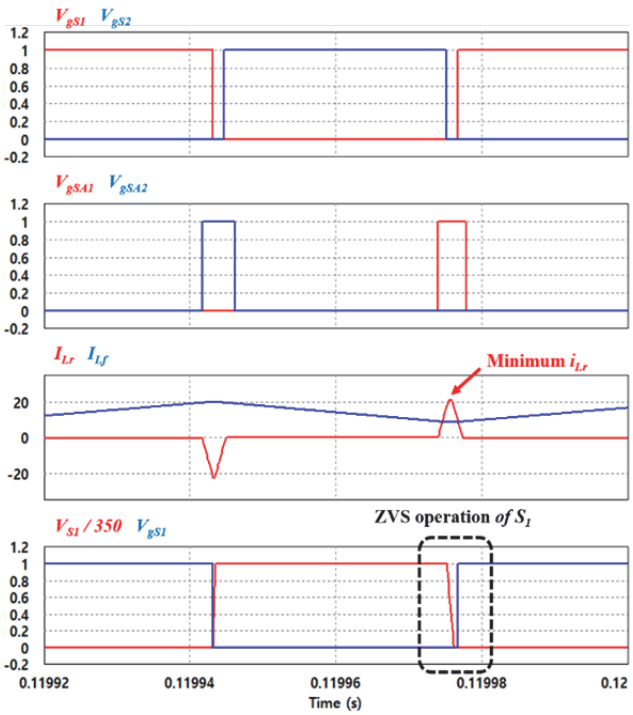


Fig. 10. Simulation results during buck operation.

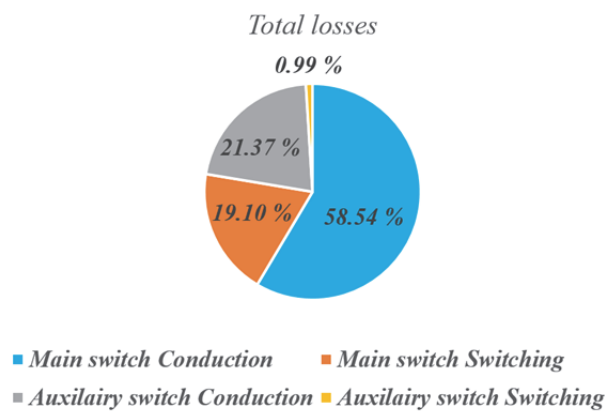


Fig. 11. Analysis of the power loss from the switches.

as shown in this figure. When S_1 is turned off, I_{Lr} charges C_{r1} and discharges C_{r2} during the dead-time. The ZVS condition is satisfied when V_{Cr2} is zero, as shown in the figure. In this mode, S_{A1} is operated for the balancing control.

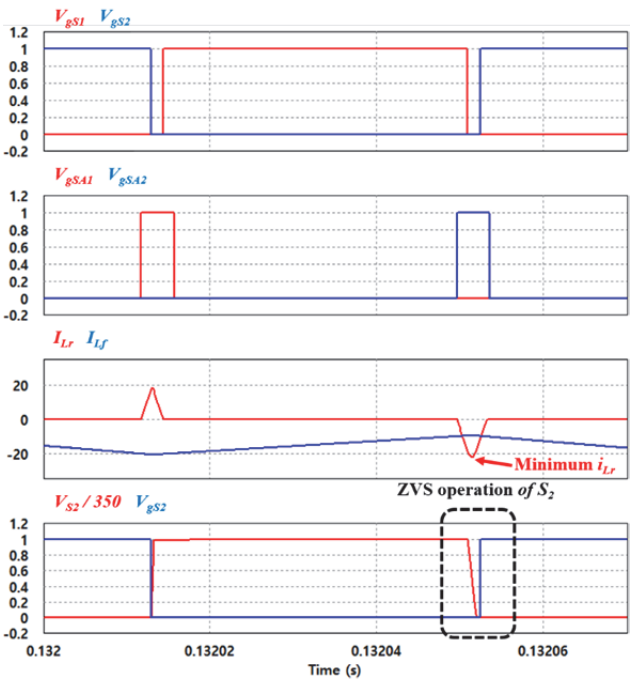


Fig. 12. Simulation results during boost operation.

VII. Experiment Results

An experiment was implemented on a 3-kW prototype ZVS converter to verify the effectiveness of the proposed topology and control algorithm. The experimental setup is shown in Fig. 13. The experimental setup was composed of a half-bridge BDC with an auxiliary circuit, gate driver modules, a control board, an ADC sensing circuit, and a switching mode power supply (SMPS). The experimental parameters were the same as those in Table I. Table III shows the specification of the main and the auxiliary switches. The proposed ZVS BDC was utilized in both buck and boost operations. In order to reduce the turn-off loss of the main switches, an additional resonant capacitor was connected in parallel to the main switches. VMO60-05Fs from IXYS were used for the auxiliary switches. The buck and boost operations can be distinguished by the direction of the filter inductor current. A positive current of the filter inductor implies buck operation. The opposite case implies boost operation.

Fig. 14 shows I_{Lf} and I_{Lr} according to the gate signals in the two modes. The operation mode is distinguished according to the gate signal of the auxiliary switch and the direction of I_{Lf} and I_{Lr}. As shown in Fig. 14(a), in the buck mode, I_{Lr} flows in the positive direction during the turn-on state of S_{A1}. Furthermore, I_{Lf} flows in the positive direction. On the other hand, when S_{A2} is turned on, I_{Lr} flows in the negative direction. In the boost mode, I_{Lf} flows in the negative direction and I_{Lr} flows in the positive direction when S_{A1} is in the on state as shown in Fig. 14(b).

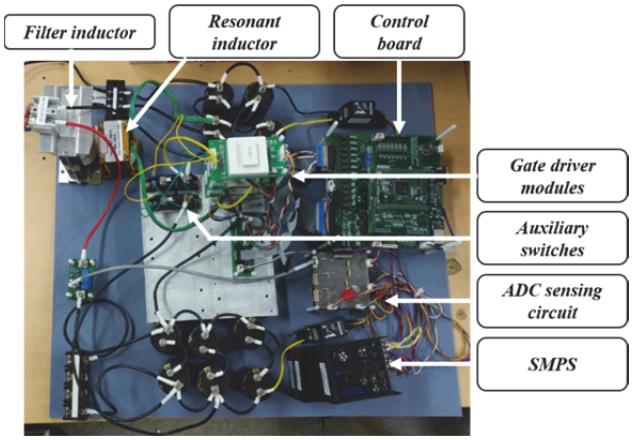


Fig. 13. Experimental setup.

TABLE III
Specifications of the Main and Auxiliary Switches

Part Number	Parameter	Value
VMO 60-05F (MOSFET)	I_D (25℃)	60 A
	C_{oss}	1.35 nF
	V_{DSS}	500 V
	V_{SD}	1.5 V

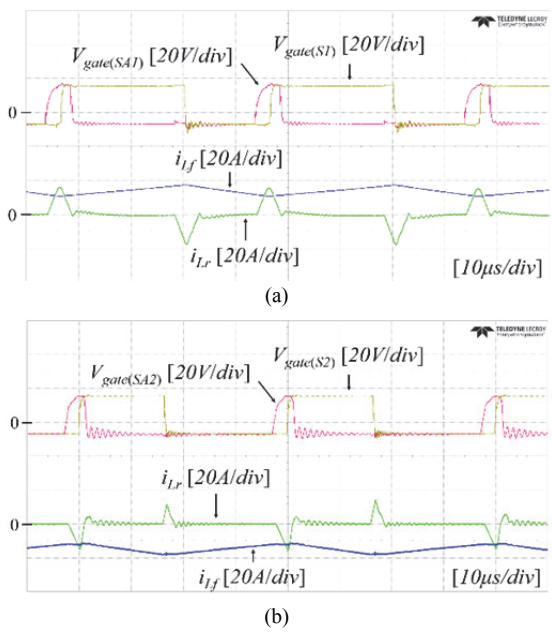
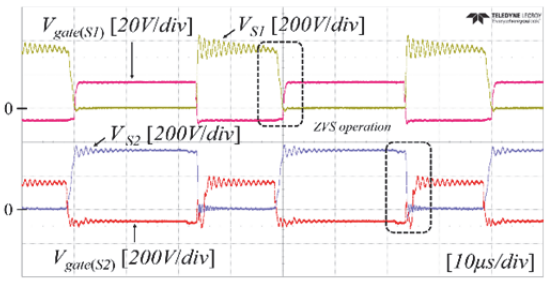
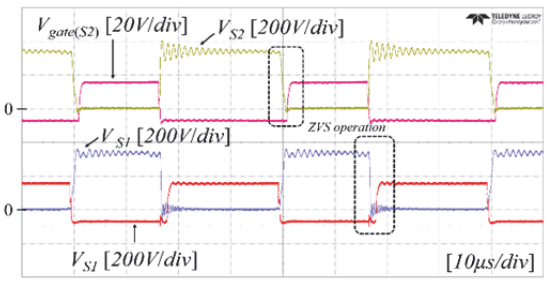


Fig. 14. I_{Lf} and I_{Lr} with gate signals depending on the operation mode: (a) Buck mode; (b) Boost mode.

Fig. 15 represents the ZVS turn-on operation of the main switches in the buck and boost modes. S_1 and S_2 perform the ZVS operation regardless of the operation mode. The energy of C_{r1} is fully discharged before V_{gS1} is turned on, as shown in Fig. 15(a). For this reason, the ZVS condition of S_1 is ensured by the resonance. For S_2, the energy of C_{r2} is discharged before S_2 is turned on during the dead-time. Therefore, S_2 also performs the ZVS turn-on in the buck mode. In the boost mode, the ZVS turn-on of S_2 is possible in the same manner

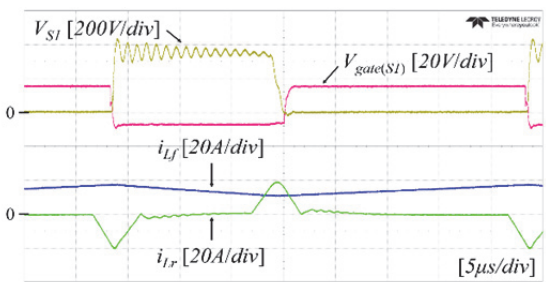


(a)

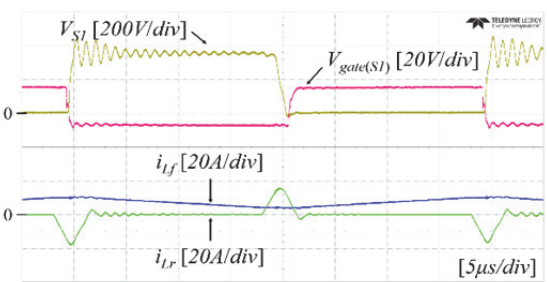


(b)

Fig. 15. ZVS turn-on operations of the main switches: (a) Buck mode; (b) Boost mode.



(a)



(b)

Fig. 16. ZVS operations under variation of the load condition in buck operation: (a) 100 % load condition and (b) 50 % load condition.

as in the buck mode as shown in Fig. 15(b).

Fig. 16 shows the ZVS operation of S_1 when a variation of the load occurs in the buck mode. The peak value of i_{Lr} is almost 20 A in the 100 % load condition as shown in Fig. 16(a). Comparing Figs. 16(a) and 16(b) shows that the peak value of i_{Lr} decreases to 12 A at the 50 % load condition. Therefore, the ZVS operation of the main switches can be achieved because the optimal current is injected according to the load condition.

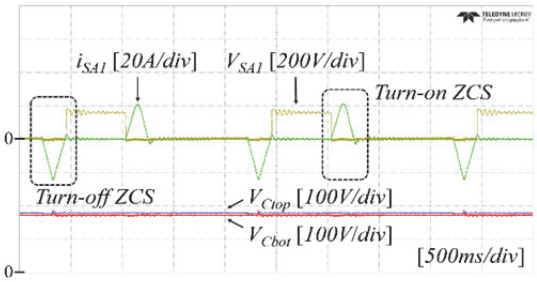


Fig. 17. ZCS operation of the auxiliary switches in the buck mode.

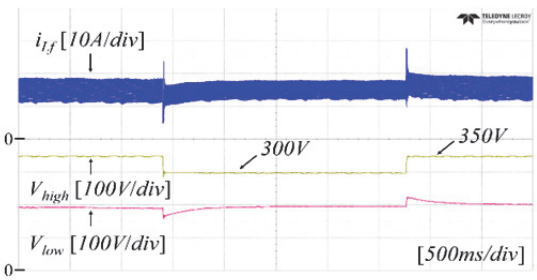


Fig. 18. Variation of the input voltage in the buck mode.

Fig. 17 shows the ZCS operation of the auxiliary switch and the voltage of C_{top} and C_{bot} in the buck mode. The ZCS turn-on of S_{A1} is achieved because the current is zero when S_{A1} is triggered. The ZCS turn-off operation is also possible because S_{A1} is triggered after the current of S_{A1} reaches zero. In boost operation, the ZCS turn-on and turn-off operations of S_{A2} are performed in the same manner as in buck operation. In addition, Fig. 17 shows the voltage of the auxiliary capacitors in buck operation. Since the voltage of C_{bot} is decreased when compared with half of V_{high}, the duty ratio of S_{A2} is increased 1 %. In the opposite case, the duty ratio of S_{A2} is decreased in the same manner. The voltage of the capacitors, as shown in Fig. 17, is maintained at 175 V, which is half of V_{high}, by using the proposed control scheme.

Fig. 18 shows the input voltage variation at a fixed load in buck operation. As shown in Fig. 18, the input voltage varies from 350 V to 300 V and from 300 V to 350 V. Despite the variations of the input voltage, the output voltage is kept constant.

Figs. 19 and 20 indicate an efficiency comparison between the conventional ZVS converter proposed in [11] and the proposed ZVS converter in the buck and boost operations. The efficiency of the proposed ZVS converter is higher than that of the conventional ZVS converter under the wide-load condition as shown in Fig. 19 and Fig. 20. The conduction loss of the main switches increases due to the large current ripple of the filter inductor in the conventional ZVS converter. On the other hand, in the proposed control method, because the minimum resonant inductor current required for ZVS operation is used during a short time, the conduction losses of the main switches and auxiliary switches can be reduced

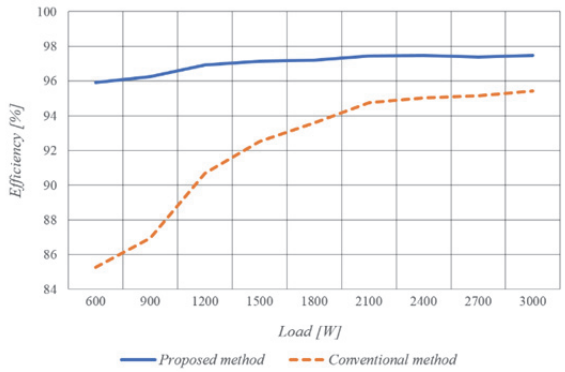


Fig. 19. Experimental efficiency graph in the buck mode.

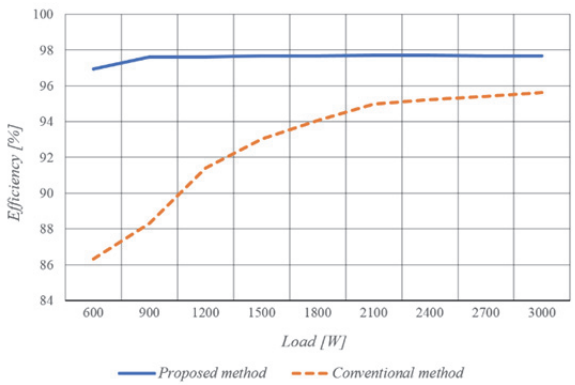


Fig. 20. Experimental efficiency graph in the boost mode.

when compared with those of the conventional ZVS converter. In particular, the improvement of efficiency is greatly increased under light load conditions.

VIII. Conclusions

In this paper, a ZVS BDC with an auxiliary circuit is proposed. The auxiliary circuit is composed of a resonant inductor, a back-to-back switch and two capacitors. The auxiliary circuit is connected between the middle of the main switches S_1 and S_2 and the middle of V_{high}. By adjusting the turn-on time of the auxiliary switch from a look-up table reference depending on the load current, the minimum resonant inductor current is supplied to the main switches for ZVS operation. Therefore, the ZVS operation of the main switches is ensured in both the buck and boost operations. As a result, the proposed dc-dc converter can improve efficiency by achieving soft switching for wide-load conditions. The proposed topology and control method are verified by simulation and experimental results.

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